Cmos Plls And Vcos For 4g Wireless 1st Edition By Aktas Adem Ismail Mohammed 2004 Hardcover

Content-Based Video RetrievalDigital Circuits and SystemsHigh-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOSLow Power UWB CMOS Radar SensorsCMOS Fractional-N SynthesizersLinear Integrated Circuit D.A.T.A. BookPhaselock TechniquesDesign of High-performance VCOs for CommunicationsLow-Power High-Speed ADCs for Nanometer CMOS IntegrationDesign of CMOS Phase-Locked LoopsIEEE International Conference on Electronics, Circuits and SystemsCMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data CommunicationsTimer/Generator Circuits ManualLow Power RF Circuit Design in Standard CMOS TechnologyNanoelectronic Mixed-Signal System DesignProceedings of the IEEE 1995 Custom Integrated Circuits ConferenceWireless CMOS Frequency Synthesizer DesignIEEE Circuits & DevicesProceedingsIndex to IEEE PublicationsIntegrated Circuits for Wireless CommunicationsIEICE Transactions on ElectronicsCMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz ApplicationsLow Power VCO Design in CMOSCMOS Nanoelectronics: Analog and RF VLSI CircuitsGPS and Galileo: Dual RF Front-end receiver and Design, Fabrication, & TestPCB Design for Real-World EMI ControlPll Performance, Simulation and DesignAll-Digital Frequency

Synthesizer in Deep-Submicron CMOSDesign Methodology for RF CMOS Phase Locked LoopsMicroCMOS DesignAdvances in Computing, Communication and ControlCMOS PLL Synthesizers: Analysis and DesignDesign of High-Performance CMOS Voltage-Controlled OscillatorsLNA-ESD Co-Design for Fully Integrated CMOS Wireless ReceiversCMOS PLLs and VCOs for 4G WirelessFully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power ApplicationsDesign of High-Performance CMOS Voltage-Controlled OscillatorsProceedings of the IEEE 1999 Custom Integrated Circuits ConferenceDesign of CMOS RF Integrated Circuits and Systems

Content-Based Video Retrieval

Fully-depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications addresses the problem of reducing the supply voltage of conventional circuits for ultralow-power operation and explains power-efficient MTCMOS circuit design for FD-SOI devices at a supply voltage of 0.5 V. The topics include the minimum required knowledge of the fabrication of SOI substrates; FD-SOI devices and the latest developments in device and process technologies; and ultralow-voltage circuits, such as digital circuits, analog/RF circuits, and DC-DC converters. Each ultra-low-power technique related to devices and circuits is fully explained using figures to help understanding.

Digital Circuits and Systems

Design of High-Performance CMOS Voltage-Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail-to-rail switching has to be achieved to minimize phase noise. Additionally, in conventional design the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor (Qeff) for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present.

High-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOS

This book provides the most comprehensive and in-depth coverage of the latest circuit design developments in RF CMOS technology. It is a practical and cutting-

edge guide, packed with proven circuit techniques and innovative design methodologies for solving challenging problems associated with RF integrated circuits and systems. This invaluable resource features a collection of the finest design practices that may soon drive the system-on-chip revolution. Using this book's state-of-the-art design techniques, one can apply existing technologies in novel ways and to create new circuit designs for the future.

Low Power UWB CMOS Radar Sensors

Timer/Generator Circuits Manual is an 11-chapter text that deals mainly with waveform generator techniques and circuits. Each chapter starts with an explanation of the basic principles of its subject followed by a wide range of practical circuit designs. This work presents a total of over 300 practical circuits, diagrams, and tables. Chapter 1 outlines the basic principles and the different types of generator. Chapters 2 to 9 deal with a specific type of waveform generator, including sine, square, triangular, sawtooth, and special waveform generators pulse. These chapters also include pulse generator, time IC generator, and waveform synthesizer circuits. Chapter 10 examines the characteristics of phase-locked loop circuits, while Chapter 11 looks into the miscellaneous applications of the ubiquitous "555" timer type of integrated circuit. The appendix presents a number of useful waveform generator design charts, as an aid to those readers who wish to design or modify generator circuits to their own specifications.

This book will prove useful to practical design engineers, technicians, experimenters, and electronics students.

CMOS Fractional-N Synthesizers

Design of High-Performance CMOS Voltage-Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail-to-rail switching has to be achieved to minimize phase noise. Additionally, in conventional design the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor (Qeff) for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present.

Linear Integrated Circuit D.A.T.A. Book

Phaselock Techniques

While the throughput of microprocessor systems tends to increase as a result of ongoing technology scaling and the advent of multi-core systems, the off-chip I/O communication bandwidth emerges as one of the potential bottlenecks that limit overall performance. In order to alleviate the communication speed constraints, optical data communication interfaces move ever closer to the processor core. It is widely expected that future generation digital systems will increasingly rely on chip-to-chip and board-to-board optical data communications for higher bandwidth and better noise immunity. This book focuses on optical communications for short and very short distance applications and discusses the monolithic integration of optical receivers with processing elements in standard CMOS technologies. CMOS Multi-Channel Single-Chip Receivers for Multi-Gigabit Optical Data Communications provides the reader with the necessary background knowledge to fully understand the trade-offs in short-distance communication receiver design and presents the key issues to be addressed in the development of such receivers in CMOS technologies. Moreover, novel design approaches are presented. A system-level design methodology allows for the impact analysis of different block specifications and system-wide design optimization. Statistical models are used for design space exploration in the scope of jitter tolerance analysis of clock recovery circuits. CMOS Multi-Channel Single-Chip Receivers for Multi-Gigabit Optical Data Communications is required reading for practicing engineers and researchers in the field of short-

distance optical communications and optical CMOS receiver design.

Design of High-performance VCOs for Communications

CMOS Cellular Receiver Front-Ends: From Specification to Realization deals with the design of the receive path of a highly-integrated CMOS cellular transceiver for the GSM-1800 cellular system. The complete design trajectory is covered, starting from the documents describing the standard down to the systematic development of CMOS receiver ICs that comply to the standard. The design of CMOS receivers is tackled at all abstraction levels: from architecture level, via circuit level, down to the device level, and the other way around. Different receiver architectures are compared with respect to integratability, achievable performance and required building block specifications. The requirements of the GSM-1800 standard are mapped onto a set of measurable specifications for a highly-integrated low-IF receiver and distributed among the different building blocks. Several circuit topologies are presented that realize the main functions of the receive path. The dynamics of the elementary specifications of these circuits are explained in terms of the operating point of the involved devices. Wherever possible, this is done using analytical expressions. Based on these insights, detailed sizing procedures are developed to systematically size these RF circuits for a set of specifications. The feasibility of meeting the requirements of today's high-end cellular standards is demonstrated in a mainstream submicron CMOS technology by the development

of two highly-integrated GSM-1800 receivers. The theoretical core of the book discusses the fundamental and more advanced aspects of RF CMOS design. It focuses specifically on all aspects of the design of high-performance CMOS low-noise amplifiers. Attempts are made to reconcile the analog designer's and the RF designer's point of view on how to look at submicron CMOS transistors. Special attention is given to the fallacies and pitfalls of input matching in a CMOS context. A methodology for the systematic design of CMOS low-noise amplifiers is presented which is based on a bank of analytical equations for all important LNA specifications. The method is validated by the design of a low power, extremely low noise CMOS GPS LNA.

Low-Power High-Speed ADCs for Nanometer CMOS Integration

This work covers the design of CMOS fully integrated low power low phase noise voltage controlled oscillators for telecommunication or datacommuni- tion systems. The need for low power is obvious, as mobile wireless telecommunications are battery operated. As wireless telecommunication systems use oscillators in frequency synthesizers for frequency translation, the selectivity and signal to noise ratio of receivers and transmitters depend heavily on the low phase noise performance of the implemented oscillators. Datacommunication s- tems need low jitter, the time-domain equivalent of low phase noise, clocks for data detection and recovery. The power consumption is less critical. The need for multi-band and multi-

mode systems pushes the high-integration of telecommunication systems. This is o?ered by sub-micron CMOS feat- ing digital ?exibility. The recent crisis in telecommunication clearly shows that mobile hand-sets became mass-market high-volume consumer products, where low-cost is of prime importance. This need for low-cost products - livens tremendously research towards CMOS alternatives for the bipolar or BiCMOS solutions in use today.

Design of CMOS Phase-Locked Loops

Covering both the classical and emerging nanoelectronic technologies being used in mixed-signal design, this book addresses digital, analog, and memory components. Winner of the Association of American Publishers' 2016 PROSE Award in the Textbook/Physical Sciences & Mathematics category. Nanoelectronic Mixed-Signal System Design offers professionals and students a unified perspective on the science, engineering, and technology behind nanoelectronics system design. Written by the director of the NanoSystem Design Laboratory at the University of North Texas, this comprehensive guide provides a large-scale picture of the design and manufacturing aspects of nanoelectronic-based systems. It features dual coverage of mixed-signal circuit and system design, rather than just digital or analog-only. Key topics such as process variations, power dissipation, and security aspects of electronic system design are discussed. Top-down analysis of all stages--from design to manufacturing Coverage of current and developing

nanoelectronic technologies--not just nano-CMOS Describes the basics of nanoelectronic technology and the structure of popular electronic systems Reveals the techniques required for design excellence and manufacturability

IEEE International Conference on Electronics, Circuits and Systems

Design State-of-the-Art GPS/Galileo Dual RF Receivers This authoritative guide walks you through the process of designing, fabricating, and testing a highly integrated, low-noise, low-power, and low-cost RF front-end for GPS and Galileo, the leading satellite-based global navigation systems. Everything from standards analysis to characterization of the design is covered in the book. GPS & Galileo focuses on developing seamlessly interoperable receivers that can access the wide variety of new services offered by these systems, such as increased service availability, centimeter-sensitive accuracy, emergency management, and data confidentiality. By the end of the book, you will have a prototype that achieves peak performance in terms of gain, NF, and current consumption, making it suitable for any high-accuracy, portable application. Discover how to: Determine the specifications of an interoperable dual GPS/Galileo RF front-end Design all RFIC blocks, including the receiver chain, PLL, control logic, and PADs Select the required external components Implement optimal floor planning Perform validation

testing of the integrated RF front-end Understand real-world fields of application Gauge the performance of the front-end within a receiver linked to a full-solution platform

CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications

Low Power UWB CMOS Radar Sensors deals with the problem of designing low cost CMOS radar sensors. The radar sensor uses UWB signals in order to obtain a reasonable target separation capability, while maintaining a maximum signal frequency below 2 GHz. This maximum frequency value is well within the reach of current CMOS technologies. The use of UWB signals means that most of the methodologies used in the design of circuits and systems that process narrow band signals, can no longer be applied. Low Power UWB CMOS Radar Sensors provides an analysis between the interaction of UWB signals, the antennas and the processing circuits. This analysis leads to some interesting conclusions on the types of antennas and types of circuits that should be used. A methodology to compare the noise performance of UWB processing circuits is also derived. This methodology is used to analyze and design the constituting circuits of the radar transceiver. In order to validate the design methodology a CMOS prototype is designed and experimentally evaluated.

Timer/Generator Circuits Manual

This modern, pedagogic textbook from leading author Behzad Razavi provides a comprehensive and rigorous introduction to CMOS PLL design, featuring intuitive presentation of theoretical concepts, extensive circuit simulations, over 200 worked examples, and 250 end-of-chapter problems. The perfect text for senior undergraduate and graduate students.

Low Power RF Circuit Design in Standard CMOS Technology

Nanoelectronic Mixed-Signal System Design

Proceedings of the IEEE 1995 Custom Integrated Circuits Conference

Low-Power High-Speed ADCs for Nanometer CMOS Integration is about the design and implementation of ADC in nanometer CMOS processes that achieve lower power consumption for a given speed and resolution than previous designs, through architectural and circuit innovations that take advantage of unique

features of nanometer CMOS processes. A phase lock loop (PLL) clock multiplier has also been designed using new circuit techniques and successfully tested. 1) A 1.2V, 52mW, 210MS/s 10-bit two-step ADC in 130nm CMOS occupying 0.38mm2. Using offset canceling comparators and capacitor networks implemented with small value interconnect capacitors to replace resistor ladder/multiplexer in conventional sub-ranging ADCs, it achieves 74dB SFDR for 10MHz and 71dB SFDR for 100MHz input. 2) A 32mW, 1.25GS/s 6-bit ADC with 2.5GHz internal clock in 130nm CMOS. A new type of architecture that combines flash and SAR enables the lowest power consumption, 6-bit >1GS/s ADC reported to date. This design can be a drop-in replacement for existing flash ADCs since it does require any post-processing or calibration step and has the same latency as flash. 3) A 0.4ps-rms-jitter (integrated from 3kHz to 300MHz offset for >2.5GHz) 1-3GHz tunable, phase-noise programmable clock-multiplier PLL for generating sampling clock to the SAR ADC. A new loop filter structure enables phase error preamplification to lower PLL in-band noise without increasing loop filter capacitor size.

Wireless CMOS Frequency Synthesizer Design

The recent boom in the mobile telecommunication market has trapped the interest of almost all electronic and communication companies worldwide. New applications arise every day, more and more countries are covered by digital cellular systems and the competition between the several providers has caused prices to drop

rapidly. The creation of this essentially new market would not have been possible without the ap pearance of small, low-power, high-performant and certainly low-cost mobile termi nals. The evolution in microelectronics has played a dominant role in this by creating digital signal processing (DSP) chips with more and more computing power and com bining the discrete components of the RF front-end on a few ICs. This work is situated in this last area, i. e. the study of the full integration of the RF transceiver on a single die. Furthermore, in order to be compatible with the digital processing technology, a standard CMOS process without tuning, trimming or post-processing steps must be used. This should flatten the road towards the ultimate goal: the single chip mobile phone. The local oscillator (LO) frequency synthesizer poses some major problems for integration and is the subject of this work. The first, and also the largest, part of this text discusses the design of the Voltage Controlled Oscillator (VCO). The general phase noise theory of LC-oscillators is pre sented, and the concept of effective resistance and capacitance is introduced to char acterize and compare the performance of different LC-tanks.

IEEE Circuits & Devices

Proceedings

Electrical Engineering Integrated Circuits for Wireless Communications High-frequency integrated circuit design is a booming area of growth that is driven not only by the expanding capabilities of underlying circuit technologies like CMOS, but also by the dramatic increase in wireless communications products that depend on them. Integrated Circuits for Wireless Communications includes seminal and classic papers in the field and is the first all-in-one resource to address this increasingly important topic. Internationally known and highly regarded in the field, editors Asad Abidi, Paul Gray, and Robert G. Meyer have meticulously compiled more than 100 papers and articles covering the very latest high-level integrated circuits techniques and solutions in use today. Integrated Circuits for Wireless Communications is devised expressly to provide IC design engineers, system architects, and integrators with a practical understanding of subjects ranging from architecture choices for integrated transceivers to actual circuit designs in all viable IC technologies, such as bipolar, CMOS, and GaAs. The papers selected represent a breadth of coverage and level of expertise that is simply unmatched in the field. Topics covered include: Radio architectures Receivers Transmitters and transceivers Power amplifiers and RF switches Oscillators Passive components Systems applications

Index to IEEE Publications

In this book, the authors outline detailed design methodology for fast frequency

hopping synthesizers for RF and wireless communications applications. There is great emphasis on fractional-N delta-sigma based phase locked loops from specifications, system analysis and architecture planning to circuit design and silicon implementation. The developed techniques in the book can help in designing very low noise, high speed fractional-N frequency synthesizers.

Integrated Circuits for Wireless Communications

IEICE Transactions on Electronics

Proper design of printed circuit boards can make the difference between a product passing emissions requirements during the first cycle or not. Traditional EMC design practices have been simply rule-based, that is, a list of rules-of-thumb are presented to the board designers to implement. When a particular rule-of-thumb is difficult to implement, it is often ignored. After the product is built, it will often fail emission requirements and various time consuming and costly add-ons are then required. Proper EMC design does not require advanced degrees from universities, nor does it require strenuous mathematics. It does require a basic understanding of the underlying principles of the potential causes of EMC emissions. With this basic understanding, circuit board designers can make trade-off decisions during

the design phase to ensure optimum EMC design. Consideration of these potential sources will allow the design to pass the emissions requirements the first time in the test laboratory. A number of other books have been published on EMC. Most are general books on EMC and do not focus on printed circuit board is intended to help EMC engineers and design design. This book engineers understand the potential sources of emissions and how to reduce, control, or eliminate these sources. This book is intended to be a 'hands-on' book, that is, designers should be able to apply the concepts in this book directly to their designs in the real-world.

CMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz Applications

LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers fits in the quest for complete CMOS integration of wireless receiver front-ends. With a combined discussion of both RF and ESD performance, it tackles one of the final obstacles on the road to CMOS integration. The book is conceived as a design guide for those actively involved in the design of CMOS wireless receivers. The book starts with a comprehensive introduction to the performance requirements of low-noise amplifiers in wireless receivers. Several popular topologies are explained and compared with respect to future technology and frequency scaling. The ESD requirements are introduced and related to the state-of-the-art protection devices

and circuits. LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers provides an extensive theoretical treatment of the performance of CMOS low-noise amplifiers in the presence of ESD-protection circuitry. The influence of the ESD-protection parasitics on noise figure, gain, linearity, and matching are investigated. Several RF-ESD co-design solutions are discussed allowing both high RF-performance and good ESD-immunity for frequencies up to and beyond 5 GHz. Special attention is also paid to the layout of both active and passive components. LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers offers the reader intuitive insight in the LNA's behavior, as well as the necessary mathematical background to optimize its performance. All material is experimentally verified with several CMOS implementations, among which a fully integrated GPS receiver front-end. The book is essential reading for RF design engineers and researchers in the field and is also suitable as a text book for an advanced course on the subject.

Low Power VCO Design in CMOS

A new and innovative paradigm for RF frequency synthesis and wireless transmitter design Learn the techniques for designing and implementing an all-digital RF frequency synthesizer. In contrast to traditional RF techniques, this innovative book sets forth digitally intensive design techniques that lead the way to the development of low-cost, low-power, and highly integrated circuits for RF functions in deep submicron CMOS processes. Furthermore, the authors

demonstrate how the architecture enables readers to integrate an RF front-end with the digital back-end onto a single silicon die using standard ASIC design flow. Taking a bottom-up approach that progressively builds skills and knowledge, the book begins with an introduction to basic concepts of frequency synthesis and then guides the reader through an all-digital RF frequency synthesizer design: Chapter 2 presents a digitally controlled oscillator (DCO), which is the foundation of a novel architecture, and introduces a time-domain model used for analysis and VHDL simulation Chapter 3 adds a hierarchical layer of arithmetic abstraction to the DCO that makes it easier to operate algorithmically Chapter 4 builds a phase correction mechanism around the DCO such that the system's frequency drift or wander performance matches that of the stable external frequency reference Chapter 5 presents an application of the all-digital RF synthesizer Chapter 6 describes the behavioral modeling and simulation methodology used in design The final chapter presents the implementation of a full transmitter and experimental results. The novel ideas presented here have been implemented and proven in two high-volume, commercial single-chip radios developed at Texas Instruments: Bluetooth and GSM. While the focus of the book is on RF frequency synthesizer design, the techniques can be applied to the design of other digitally assisted analog circuits as well. This book is a must-read for students and engineers who want to learn a new paradigm for RF frequency synthesis and wireless transmitter design using digitally intensive design techniques.

CMOS Nanoelectronics: Analog and RF VLSI Circuits

This book constitutes the refereed proceedings of the International Conference on Advances in Computing Communications and Control, ICAC3 2011, held in Mumbai, India, in January 2011. The 84 revised full papers presented were carefully reviewed and selected from 309 submissions. The papers address issues such as AI, artificial neural networks, computer graphics, data warehousing and mining, distributed computing, geo information and statistical computing, learning algorithms, system security, virtual reality, cloud computing, service oriented architecture, semantic web, coding techniques, modeling and simulation of communication systems, network architecture, network protocols, optical fiber/microwave communication, satellite communication, speech/image processing, wired and wireless communication, cooperative control, and nonlinear control, process control and instrumentation, industrial automation, controls in aerospace, robotics, and power systems.

GPS and Galileo: Dual RF Front-end receiver and Design, Fabrication, & Test

PCB Design for Real-World EMI Control

This book presents high-/mixed-voltage analog and radio frequency (RF) circuit techniques for developing low-cost multistandard wireless receivers in nm-length CMOS processes. Key benefits of high-/mixed-voltage RF and analog CMOS circuits are explained, state-of-the-art examples are studied, and circuit solutions before and after voltage-conscious design are compared. Three real design examples are included, which demonstrate the feasibility of high-/mixed-voltage circuit techniques. Provides a valuable summary and real case studies of the state-of-the-art in high-/mixed-voltage circuits and systems; Includes novel high-/mixed-voltage analog and RF circuit techniques – from concept to practice; Describes the first high-voltage-enabled mobile-TVRF front-end in 90nm CMOS and the first mixed-voltage full-band mobile-TV Receiver in 65nm CMOS; Demonstrates the feasibility of high-/mixed-voltage circuit techniques with real design examples.

Pll Performance, Simulation and Design

A greatly revised and expanded account of phaselocktechnology The Third Edition of this landmark book presents new developmentsin the field of phaselock loops, some of which have never beenpublished until now. Established concepts are reviewed criticallyand recommendations are offered for improved formulations. The workreflects the author's own research and many years of hands-onexperience with phaselock loops. Reflecting the myriad of phaselock loops that are now found

inelectronic devices such as televisions, computers, radios, and cellphones, the book offers readers much new material, including: * Revised and expanded coverage of transfer functions * Two chapters on phase noise * Two chapters examining digital phaselock loops * A chapter on charge-pump phaselock loops * Expanded discussion of phase detectors and of oscillators * A chapter on anomalous phaselocking * A chapter on graphical aids, including Bode plots, root locusplots, and Nichols charts As in the previous editions, the focus of the book is on underlyingprinciples, which remain valid despite technological advances.Extensive references guide readers to additional information tohelp them explore particular topics in greater depth. Phaselock Techniques, Third Edition is intended for practicingengineers, researchers, and graduate students. This criticallyacclaimed book has been thoroughly updated with new information andexpanded for greater depth.

All-Digital Frequency Synthesizer in Deep-Submicron CMOS

Design Methodology for RF CMOS Phase Locked Loops

MicroCMOS Design

MicroCMOS Design covers key analog design methodologies with an emphasis on analog systems that can be integrated into systems-on-chip (SoCs). Starting at the transistor level, this book introduces basic concepts in the design of system-level complementary metal-oxide semiconductors (CMOS). It uses practical examples to illustrate circuit construction so that readers can develop an intuitive understanding rather than just assimilate the usual conventional analytical knowledge. As SoCs become increasingly complex, analog/radio frequency (RF) system designers have to master both system- and transistor-level design aspects. They must understand abstract concepts associated with large components, such as analog-to-digital converters (ADCs) and phase-locked loops (PLLs). To help readers along, this book discusses topics including: Amplifier basics & design Operational amplifier (Opamp) Data converter basics Nyquist-rate data converters Oversampling data converters High-resolution data converters PLL basics Frequency synthesis and clock recovery Focused more on design than analysis, this reference avoids lengthy equations and instead helps readers acquire a more hands-on mastery of the subject based on the application of core design concepts. Offering the needed perspective on the various design techniques for data converter and PLL design, coverage starts with abstract concepts—including discussion of bipolar junction transistors (BJTs) and MOS transistors—and builds up to an examination of the larger systems derived from microCMOS design.

Advances in Computing, Communication and Control

CMOS PLL Synthesizers: Analysis and Design

This book is intended for the reader who wishes to gain a solid understanding of Phase Locked Loop architectures and their applications. It provides a unique balance between both theoretical perspectives and practical design trade-offs. Engineers faced with real world design problems will find this book to be a valuable reference providing example implementations, the underlying equations that describe synthesizer behavior, and measured results that will improve confidence that the equations are a reliable predictor of system behavior. New material in the Fourth Edition includes partially integrated loop filter implementations, voltage controlled oscillators, and modulation using the PLL.

Design of High-Performance CMOS Voltage-Controlled Oscillators

CMOS Fractional-N Synthesizers starts with a comprehensive introduction to general frequency synthesis. Different architectures and synthesizer building blocks are discussed with their relative importance on synthesizer specifications. The process of synthesizer specification derivation is illustrated with the DCS-1800 standard as a general test case. The book tackles the design of fractional-N

synthesizers in CMOS on circuit level as well as system level. The circuit level focuses on high-speed prescaler design up to 12 GHz in CMOS and on fully integrated, low-phase-noise LC-VCO design. High-Q inductor integration and simulation in CMOS is elaborated and flicker noise minimization techniques are presented, ranging from bias point choice to noise filtering techniques. On a higher level, a systematic design strategy has been developed that trades off all noise contributions and fast dynamics for integrated capacitance (area). Moreover, a theoretical DeltaSigma phase noise analysis is presented, extended with a fast non-linear analysis method to accurately predict the influence of PLL non-linearities on the spectral purity of the DeltaSigma fractional-N frequency synthesizers.

LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers

Low Power Consumption is one of the critical issues in the performance of small battery-powered handheld devices. Mobile terminals feature an ever increasing number of wireless communication alternatives including GPS, Bluetooth, GSM, 3G, WiFi or DVB-H. Considering that the total power available for each terminal is limited by the relatively slow increase in battery performance expected in the near future, the need for efficient circuits is now critical. This book presents the basic techniques available to design low power RF CMOS analogue circuits. It gives

circuit designers a complete guide of alternatives to optimize power consumption and explains the application of these rules in the most common RF building blocks: LNA, mixers and PLLs. It is set out using practical examples and offers a unique perspective as it targets designers working within the standard CMOS process and all the limitations inherent in these technologies.

CMOS PLLs and VCOs for 4G Wireless

After a review of PLL essentials, this uniquely comprehensive workbench guide takes you step-by-step through operation principles, design procedures, phase noise analysis, layout considerations, and CMOS realizations for each PLL building block. You get full details on LC tank oscillators including modeling and optimization techniques, followed by design options for CMOS frequency dividers covering flip-flop implementation, the divider by 2 component, and other key factors. The book includes design alternatives for phase detectors that feature methods to minimize jitter caused by the dead zone effect. You also find a sample design of a fully integrated PLL for WLAN applications that demonstrates every step and detail right down to the circuit schematics and layout diagrams. Supported by over 150 diagrams and photos, this one-stop toolkit helps you produce superior PLL designs faster, and deliver more effective solutions for low-cost integrated circuits in all RF applications.

Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications

CMOS PLLs and VCOs for 4G Wireless is the first book devoted to the subject of CMOS PLL and VCO design for future broadband 4th generation wireless devices. These devices will be handheld-centric, requiring very low power consumption and small footprint. They will be able to work across multiple bands and multiple standards covering WWAN (GSM,WCDMA) ,WLAN(802.11 a/b/g) and WPAN(Bluetooth) with different modulations, channel bandwidths , phase noise requirements ,etc. As such, this book discusses design, modeling and optimization techniques for low power fully integrated broadband PLLs and VCOs in deep submicron CMOS. First, the PLL and VCO performances are studied in the context of the chosen multi-band multi-standard, radio architecture and the adopted frequency plan. Next a thorough study of the design requirements for broadband PLL/VCO design is conducted together with modeling techniques for noise sources in a PLL and VCO focusing on optimization of integrated phase noise for multi-carrier OFDM 64-QAM type applications. Design examples for multi-standard 802.111a/b/g as well as for GSM/WCDMA are fully described and experimental results from 0.18 micron CMOS test chips have demonstrated the validity of the proposed design and optimization techniques. Equally important the work describes techniques for robust high volume production of RF radios in general and

for integrated PLL/VCO design in particular including issues such as supply sensitivity, ground bounce and calibration mechanisms. CMOS PLLS and VCOs for 4G Wireless will be of interest to graduate students in electrical and computer engineering, design managers and RFIC designers in wireless semiconductor companies.

Design of High-Performance CMOS Voltage-Controlled Oscillators

Proceedings of the IEEE 1999 Custom Integrated Circuits Conference

Thanks to the advance of semiconductor and communication technology, the wireless communication market has been booming in the last two decades. It evolved from simple pagers to emerging third-generation (3G) cellular phones. In the meanwhile, broadband communication market has also gained a rapid growth. As the market always demands hi- performance and low-cost products, circuit designers are seeking hi- integration communication devices in cheap CMOS technology. The phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and

channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converters in the analog-and-digital signal interface. This book covers the design and analysis of PLL synthesizers. It includes both fundamentals and a review of the state-of-the-art techniques. The transient analysis of the third-order charge-pump PLL reveals its locking behavior accurately. The behavioral-level simulation of PLL further clarifies its stability limit. Design examples are given to clearly illustrate the design procedure of PLL synthesizers. A complete derivation of reference spurs in the charge-pump PLL is also presented in this book. The in-depth investigation of the digital CA modulator for fractional-N synthesizers provides insightful design guidelines for this important block.

Design of CMOS RF Integrated Circuits and Systems

In-depth coverage of integrated circuit design on the nanoscale level Written by international experts in industry and academia, CMOS Nanoelectronics addresses the state of the art in integrated circuit design in the context of emerging systems. New, exciting opportunities in body area networks, wireless communications, data networking, and optical imaging are discussed. This cutting-edge guide explores emerging design concepts for very low power and describes design approaches for RF transceivers, high-speed serial links, PLL/DLL, and ADC/DAC converters. CMOS Nanoelectronics covers: Portable high-efficiency polar transmitters All-digital RF

signal generation Frequency multiplier design Tunable CMOS RF filters GaAs HBT linear power amplifier design High-speed serial I/O design CDMA-based crosstalk cancellation Delta-sigma fractional-N PLL Delay locked loops Digital clock generators Analog design in deep submicron CMOS technologies 1/f noise reduction for linear analog CMOS ICs Broadband high-resolution bandpass sigma-delta modulators Analog/digital conversion specifications for power line communication systems Digital-to-analog converters for LCDs Sub-1-V CMOS bandgap reference design And much more